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EXAMINER	
TRUONG, BAO Q	
ART UNIT	**PAPER NUMBER**
2187	5

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/866,981	Applicant(s) FREERKSEN ET AL.	
	Examiner Bao Q Truong	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9-23 and 28-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9,14,15,20-23,28,33 and 34* is/are rejected.

7)☒ Claim(s) *10-13,16-19,29-32 and 35-38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The instant application having Application No. 09/866,981 has a total of 30 claims pending in the application; there are 6 independent claims and 24 dependent claims, all of which are ready for examination by the examiner.

Information Disclosure Statement

2. As required by M.P.E.P § 609 (C), the applicant's submission of the Information Disclosure Statement, dated on 2 August 2001, is acknowledged by the examiner; and the cited reference has been considered in the examination of the claims now pending. As required by M.P.E.P § 609 C (2), a copy of the PTO-1449 initialed and dated by the examiner is attached to the instant office action.

Drawings

3. The drawings are objected to because:

Figure 7 fails to show path selection value for step **S40**.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 12 recites the limitation "said transition" in line 2-3 of the claim. There is insufficient antecedent basis for this limitation in the claim. The applicant is suggested to change this limitation to "said transition cache". Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-2, 14, 20-21, and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Ebrahim et al. (U.S. Patent No. 5,905,998).

Referring to claim 1, Ebrahim teaches a method for increasing communication efficiency in a multi-processor system (see figure 1 and "abstract"), comprising:

(1) snooping, at a processor having a transition cache (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2) and at least one level of cache associated therewith (see figure 1 and 7: element 130), a first command on a system bus, said system bus providing communication between processors in said multi-processor system, wherein said first command requesting invalidation of a cache line as monitoring a "ReadToOwn" request (see column 35: line 48) or a "WriteInvalidate" request (see column 37: line 59) sent by another UPA master;

(2) generating a second command in response to said first command at one of said levels of cache which stores said cache line if a memory image coherency state of said cache line indicates that said cache line includes modified data, said second command instructing that said cache line be castback as generating a "Writeback" request to write a "Dirty Victim" back to main memory (see column 4: lines 18-25, and column 36: line 62);

(3) transferring said second command and said cache line from said one of said levels of cache to said transition cache in response to said first command as a command and its associated data are transferred to a queue in the interface (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(4) invalidating said cache line in each level of cache associated with said processor that stores said cache line as the System Controller requests all port invalidate the datum (see column 39: lines 4-8);

(5) snooping a system response to said first command at said processor as monitoring the System Controller's response to a "ReadToOwn" request or a "WriteInvalidate" request; and

(6) processing said second command at said processor based on said system response to said first command as writeback is cancelled (see column 21: lines 56-67, and column 37: lines 16-24) if the System Controller responds to a "ReadToOwn" request or a "WriteInvalidate" request with an "Invalidate" request (see column 38: line 59) or a "CopybackInvalidate" request (see column 40: line 18).

As to claim 2, Ebrahim further teaches that said processing step discards said second command and said cache line from said transition cache when said system response to said first command is not a retry as writeback is cancelled (see column 21: lines 56-67, and column 37: lines 16-24) if the System Controller responds to a "ReadToOwn" request or a "WriteInvalidate" request with an "Invalidate" request or a "CopybackInvalidate" request.

Referring to claim 14, Ebrahim teaches a method for increasing communication efficiency in a multi-processor system (see figure 1 and "abstract"), comprising:

(1) receiving, at a processor, a first command on a system bus, said system bus providing communication between processors in said multi-processor system, said first command requesting a cache line as receiving a "CopybackInvalidate" request (see column 40: line 18) which the System Controller sends to the ports containing said cache line in response to a "ReadToOwn" request (see column 35: line 48);

(2) transferring said requested cache line from a cache associated with said processor to a transition cache in said processor as part of a response to said first command as datum is transferred to a queue in the interface (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(3) updating a memory coherency image state associated with said cache line in each cache associated with said processor that stores said cache line as invalidating all ports containing the same datum (see column 39: lines 4-8);

(4) snooping a system response to said first command on said system bus as monitoring the System Controller's response to the requesting port which sends out the "ReadToOwn" request; and

(5) processing said requested cache line at said processor based on said system response as copying back and invalidating said cache line if the System Controller generates a S_Reply to the requesting port (see column 35: line 48).

Referring to claim 20, Ebrahim discloses a multi-processor system (see figure 1 and "abstract"), comprising:

(1) at least first and second processors (see figures 1 and 2: elements 102);

(2) a system bus providing communication between said first and second processors (see figures 1 and 2: elements 116 and 114);

(3) a bus arbiter generating system response to commands on said system bus (see figures 1 and 2: element 110); and wherein

(4) said first processor has at least one level of cache associated therewith (see figure 1 and 7: element 130), a system bus controller controlling communication between said first processor and said system bus (see figures 4 and 7: element 104), and a transition cache serving as an interface between each level of cache and said system bus controller (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(5) one of said levels of cache associated with said first processor stores a cache lines having a memory coherency image state indicating that said cache line includes modified data (see figure 10A, column 4: lines 18-28 and line 48), and generates a castback command and

transfer said castback command and a copy of said cache lines to said transition cache when said first processor snoops a first command on said system bus that requests invalidation of said cache line as generating a "Writeback" request to write a "Dirty Victim" back to main memory (see column 4: lines 18-25, and column 36: lines 62); and as a command and its associated data are transferred to a queue in the interface (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2); and

(6) each level of cache associated with said first processor that stores said cache line invalidates said cache line prior to said first processor snooping a system response to said first command as the System Controller requests all port invalidate the datum (see column 39: lines 4-8); and as monitoring the System Controller's response to a "ReadToOwn" request or a "WriteInvalidate" request.

As to claim 21, Ebrahim discloses that said transition cache discards said castback and said cache line when said system response to said first command is not a retry as writeback is cancelled (see column 21: lines 56-67, and column 37: lines 16-24) if the System Controller responds to a "ReadToOwn" request or a "WriteInvalidate" request with an "Invalidate" request or a "CopybackInvalidate" request.

Referring to claim 33, Ebrahim discloses a multi-processor system (see figure 1 and "abstract"), comprising:

(1) at least first and second processors (see figures 1 and 2: elements 102);

(2) a system bus providing communication between said first and second processors (see figures 1 and 2: elements 116 and 114);

(3) a bus arbiter generating system response to commands on said system bus (see figures 1 and 2: element 110); and wherein

(4) said first processor has at least one cache associated therewith (see figure 1 and 7: element 130), a system bus controller controlling communication between said first processor and said system bus (see figures 4 and 7: element 104), and a transition cache controlling and tracking communication between each cache and said system bus controller (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(5) said first processor receives a first command on said system bus requesting a cache line as receiving a "CopybackInvalidate" request (see column 40: line 18) which the System Controller sends to the ports containing said cache line in response to a "ReadToOwn" request (see column 35: line 48);

(6) one of said caches associated with said first processor that stores said requested cache line copies said requested cache line to said transition cache as part of a response to said first command as datum is transferred to a queue in the interface (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(7) each cache associated with said first processor, that stores said requested cache line, updates a memory coherency image state associated with said requested cache line prior to

snooping a system response to said first command as invalidating all ports containing the same datum (see column 39: lines 4-8); and

(8) said first processor snoops said system response on said system bus to said first command, and process said requested cache line based on said system response as copying back and invalidating said cache line if the System Controller generates a S_Reply to the requesting port (see column 35: line 48).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3-4, 15, 22-23, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebrahim et al. (U.S. Patent No. 5,905,998).

As to claims 3 and 4, Ebrahim teaches that said processing step discards said second command and said cache line from said transition cache when said system response to said first command is not a retry as writeback is cancelled (see column 21: lines 56-67, and column 37: lines 16-24) if the System Controller responds to a "ReadToOwn" request or a "WriteInvalidate" request with an "Invalidate" request or a "CopybackInvalidate" request.

However, Ebrahim does not clearly teach that said processing step converts said second command to a third command in said transition cache if said system response to said first command is a retry, said third command requesting said cache line be stored in a main memory of said multi-processor system.

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the method taught by Ebrahim so that said processing step converts said second command to a third command in said transition cache if said system response to said first command is a retry, said third command requesting said cache line to be stored in main memory of said multi-processor system. This would have been obvious because Ebrahim teaches that "a dirty victim must normally be written back to main memory, except that in the present invention the write back can be cancelled if the same data block is invalidated by another data processor prior to the writeback transaction becoming active" (see column 4: lines 18-25).

As to claim 15, Ebrahim teaches processing said requested cache line at said processor based on said system response as copying back and invalidating said cache line if the System Controller generates a S_Reply to the requesting port (see column 35: line 48).

However, Ebrahim does not clearly teach said processing step outputs said requested cache line on said system bus when said system response to said first command is not a retry.

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the method taught by Ebrahim so that said processing step outputs said requested cache line on said system bus when said system response to said first

command is not a retry. This would have been obvious because, if a request is responded with a retry, data should be sent out only when the transaction is taken placed, thereby the bus is free for other transaction.

As to claims 22 and 23, Ebrahim discloses that said transition cache discards said castback and said cache line when said system response to said first command is not a retry as writeback is cancelled (see column 21: lines 56-67, and column 37: lines 16-24) if the System Controller responds to a "ReadToOwn" request or a "WriteInvalidate" request with an "Invalidate" request or a "CopybackInvalidate" request.

However, Ebrahim does not clearly disclose that said transition cache converts said castback command to a second command if said system response to said first command is a retry, said second command requesting said cache line be stored in a main memory of said multi-processor system.

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the system taught by Ebrahim so that said transition cache converts said castback command to a second command if said system response to said first command is a retry, said second command requesting said cache line be stored in a main memory of said multi-processor system. This would have been obvious because Ebrahim discloses that "a dirty victim must normally be written back to main memory, except that in the present invention the write back can be cancelled if the same data block is invalidated by another data processor prior to the writeback transaction becoming active" (see column 4: lines 18-25).

As to claim 34, Ebrahim disclose that said first processor snoops said system response on said system bus to said first command, and process said requested cache line based on said system response as copying back and invalidating said cache line if the System Controller generates a S_Reply to the requesting port (see column 35: line 48).

However, Ebrahim does not clearly disclose said first processor outputs said requested cache line on said system bus when said system response to said first command is not a retry.

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the system taught by Ebrahim so that said first processor outputs said requested cache line on said system bus when said system response to said first command is not a retry. This would have been obvious because, if a request is responded with a retry, data should be sent out only when the transaction is taken placed, thereby the bus is free for other transaction.

9. Claims 9 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebrahim et al. (U.S. Patent No. 5,905,998) in view of Boddu et al. (U.S. Patent No. 5,974,511).

Referring to claim 9, Ebrahim teaches a method for increasing communication efficiency in a multi-processor system (see figure 1 and "abstract"), comprising:

(1) storing a non-exclusive command associated with a real address in a transition cache of a processor as storing a "Writeback" request for writing back a dirty victimized block to main memory (see column 4: lines 18-25, and column 36: line 62) in a queue in the interface (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(2) snooping, at said processor, a command on a system bus providing communication between processors in said multi-processor system, said snooped command being associated with said real address as monitoring the System Controller's response to "ReadToOwn" request (see column 35: line 48) or a "WriteInvalidate" request (see column 37: line 59) sent by another UPA master.

However, Ebrahim does not teach steps of:

(3) determining, at said transition cache, whether data has started to arrive at said transition cache in response to said non-exclusive command; and

(4) generating a snoop response at said transition cache to said snooped command based on a result of said determining step.

Boddu teaches a method for increasing communication efficiency similar to that of Ebrahim. Boddu further teaches steps of:

(3) determining, at said transition cache, whether data has started to arrive at said transition cache in response to said non-exclusive command as a snoop logic circuit checks a bus cache for a hit (valid data is available) (see figure 4, and column 3: lines 43-51); and

(4) generating a snoop response at said transition cache to said snooped command based on a result of said determining step as accessing and sending out data from the bus cache if cache hit; otherwise causing the interface to assert a retry operation on the bus (see figure 4, column 3: lines 51-55, and column 4: lines 1-8).

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to include steps (3) and (4) mentioned above, in the method taught by Ebrahim. This would have been obvious because Ebrahim teaches that an incoming transaction

for accessing a data block that maps to the same cache line as pending, previously activated transaction, will be blocked until the pending transaction that maps to the same cache line is completed (see column 2: lines 65-67 and column 3: lines1-2). Moreover, Boddu teaches checking if data is available at the bus cache so data can be immediately provided; otherwise a retry operation is asserted to free the bus for other transaction, thereby increasing the bandwidth of the bus (see column 2: lines 10-28).

Referring to claim 28, Ebrahim discloses a multi-processor system (see figure 1 and "abstract"), comprising:

(1) at least first and second processors (see figures 1 and 2: elements 102);

(2) a system bus providing communication between said first and second processors (see figures 1 and 2: elements 116 and 114);

(3) a bus arbiter generating system response to commands on said system bus (see figures 1 and 2: element 110); and wherein

(4) said first processor has at least one level of cache associated therewith (see figure 1 and 7: element 130), a system bus controller controlling communication between said first processor and said system bus (see figures 4 and 7: element 104), and a transition cache controlling and tracking communication between each level of cache and said system bus controller (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(5) a non-exclusive command associated with a real address is stored in a transition cache of a processor as storing a "Writeback" request for writing back a dirty victimized block to main

memory (see column 4: lines 18-25, and column 36: line 62) in a queue in the interface (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(6) said first processor snoops a command on said system bus, said snooped command being associated with said real address as monitoring the System Controller's response to "ReadToOwn" request (see column 35: line 48) or a "WriteInvalidate" request (see column 37: line 59) sent by another UPA master.

However, Ebrahim does not disclose:

(3) said transition cache determines whether data has started to arrive at said transition cache in response to said non-exclusive command; and

(4) said first processor generates a snoop response to said snooped command based on said determination.

Boddu discloses a system for increasing communication efficiency similar to that of Ebrahim. Boddu further discloses:

(3) said transition cache determines whether data has started to arrive at said transition cache in response to said non-exclusive command as a snoop logic circuit checks a bus cache for a hit (valid data is available) (see figure 4, and column 3: lines 43-51); and

(4) said first processor generates a snoop response to said snooped command based on said determination as accessing and sending out data from the bus cache if cache hit; otherwise causing the interface to assert a retry operation on the bus (see figure 4, column 3: lines 51-55, and column 4: lines 1-8).

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to include limitation (5) mentioned above, in the system taught by

Ebrahim. This would have been obvious because Ebrahim teaches that an incoming transaction for accessing a data block that maps to the same cache line as pending, previously activated transaction, will be blocked until the pending transaction that maps to the same cache line is completed (see column 2: lines 65-67 and column 3: lines1-2). Moreover, Boddu teaches checking if data is available at the bus cache so data can be immediately provided; otherwise a retry operation is asserted to free the bus for other transaction, thereby increasing the bandwidth of the bus (see column 2: lines 10-28).

Allowable Subject Matter

10. Claim 12 is objected to as being dependent upon a rejected base claim and as providing insufficient antecedent basis for one limitation in the claim (see ***Claim Objections***), but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims; and overcoming the above claim objection.

11. Claims 10-11, 13, 16-19, 29-32, and 35-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (703) 308-7090. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

BAO QUOC TRUONG
BT
Patent Examiner
October 14, 2003

Donald Sparks
Supervisory Patent Examiner
Technology Center 2100